WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a switching element formed on a semiconductor substrate;

a first interconnect layer formed on the semiconductor substrate and having a first wiring connected to one terminal of the switching element;

a ferroelectric capacitor formed on the first interconnect layer and having a first electrode connected to the one terminal of the switching element via the first wiring;

a first protective film formed on the ferroelectric capacitor and the first interconnect layer;

a second interconnect layer formed on the first protective film and having a second wiring connected to a second electrode of the ferroelectric capacitor and a first interlayer insulating film having a dielectric constant of 4 or more; and

a third interconnect layer including at least one layer formed on the second interconnect layer, the third interconnect layer having a third wiring connected to the second wiring and a second interlayer insulating film having a dielectric constant of less than 4.

2. The semiconductor device according to claim 1, wherein the first protective film contains at least one of Al_xO_y, Zr_xO_y, $Al_xSi_yO_z$, Si_xN_y, and Ti_xO_y.

3. The semiconductor device according to claim 1, further comprising a second protective film formed between the first protective film and the second interconnect layer and formed on the first protective film via a first insulating film with a dielectric constant of 4 or more.

4. The semiconductor device according to claim 3, wherein the second protective film contains at least one of Al_xO_y, Zr_xO_y, $Al_xSi_yO_z$, Si_xN_y, and Ti_xO_y.

5. The semiconductor device according to claim 1, wherein the third interconnect layer has a second insulating film formed on the second interlayer insulating film and having a dielectric constant of 4 or more.

6. The semiconductor device according to claim 1, wherein the second and third wirings are formed by a dual damascene method.

7. The semiconductor device according to claim 6, wherein the second and third wirings consist essentially of a Cu-based material.

8. The semiconductor device according to claim 1, wherein the second and third wirings are formed by a reactive ion etching method.

9. The semiconductor device according to claim 8, wherein the second and third wirings consist essentially of an Al-based material.

10. The semiconductor device according to claim 1,

wherein the first interlayer insulating film consists essentially of plasma SiO_2.

11. The semiconductor device according to claim 1, wherein the second interlayer insulating film consists essentially of $Si_xO_yC_z$.

12. The semiconductor device according to claim 1, wherein the second interlayer insulating film consists essentially of an organic material including a C_yH_y structure.

13. A semiconductor device comprising:

a switching element formed on a semiconductor substrate;

a first interconnect layer formed on the semiconductor substrate and having a first wiring connected to one terminal of the switching element;

a ferroelectric capacitor formed on the first interconnect layer and having a first electrode and a second electrode;

a first protective film formed on the ferroelectric capacitor and the first interconnect layer;

a second interconnect layer formed on the first protective film, the second interconnect layer including a second wiring having a first via plug connected to the first wiring and a second via plug connected to the first electrode of the ferroelectric capacitor, a third wiring having a third via plug connected to the second electrode of the ferroelectric

capacitor, and a first interlayer insulating film having a dielectric constant of 4 or more; and

a third interconnect layer including at least one layer formed on the second interconnect layer, the third interconnect layer having a fourth wiring connected to the third wiring and a second interlayer insulating film having a dielectric constant of less than 4.

14. The semiconductor device according to claim 13, wherein the first protective film contains at least one of Al_xO_y, Zr_xO_y, $Al_xSi_yO_z$, Si_xN_y, and Ti_xO_y.

15. The semiconductor device according to claim 13, further comprising a second protective film formed between the first protective film and the second interconnect layer and formed on the first protective film via a first insulating film with a dielectric constant of 4 or more.

16. The semiconductor device according to claim 15, wherein the second protective film contains at least one of Al_xO_y, Zr_xO_y, $Al_xSi_yO_z$, Si_xN_y, and Ti_xO_y.

17. The semiconductor device according to claim 13, wherein the third interconnect layer has a second insulating film formed on the second interlayer insulating film and having a dielectric constant of 4 or more.

18. A manufacturing method for a semiconductor

device comprising:

forming a switching element on a semiconductor substrate;

forming, on the semiconductor substrate, a first interconnect layer which has a first wiring connected to one terminal of the switching element;

forming, on the first interconnect layer, a ferroelectric capacitor which has a first electrode connected to the one terminal of the switching element via the first wiring;

forming a first protective film on the ferroelectric capacitor and the first interconnect layer;

forming, on the first protective film, a second interconnect layer which has a second wiring connected to a second electrode of the ferroelectric capacitor and a first interlayer insulating film with a dielectric constant of 4 or more; and

forming, on the second interconnect layer, a third interconnect layer which has a third wiring connected to the second wiring and a second interlayer insulating film with a dielectric constant of less than 4.

19. The manufacturing method for a semiconductor device according to claim 18, wherein the second and third wirings are formed by a dual damascene method.

20. The manufacturing method for a semiconductor device according to claim 18, wherein the second and

third wirings consist essentially of a Cu-based material.